

# OKI Semiconductor

## MSM51V4400/L/SL

1,048,576-Word × 4-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

### DESCRIPTION

The MSM51V4400/L/SL is a 1,048,576-word × 4-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM51V4400/L/SL achieves high integration, high-speed operation, and low-power consumption due to quadruple polysilicon single metal CMOS. The MSM51V4400/L/SL is available in a 26/20-pin plastic SOJ or 26/20-pin plastic TSOP. The MSM51V4400L (the low-power version) and the MSM51V4400SL (the self-refresh version) are specially designed for lower-power applications.

### FEATURES

- 1,048,576-word × 4-bit configuration
- Single 3.3 V power supply, ±0.3 V tolerance
- Input : LVTTTL compatible, low input capacitance
- Output : LVTTTL compatible, 3-state
- Refresh : 1024 cycles/16 ms, 1024 cycles/128 ms (L/SL version)
- Fast page mode, read modify write capability
- $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh, hidden refresh,  $\overline{\text{RAS}}$ -only refresh capability
- Multi-bit test mode capability
- $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self-refresh capability (SL version)
- Package options:
 

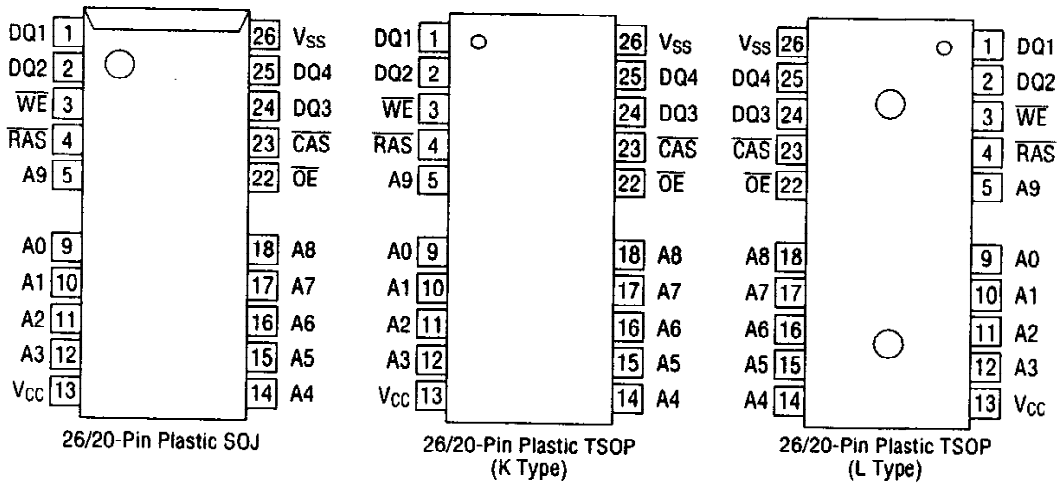
26/20-Pin 300 mil plastic SOJ	(SOJ26/20-P-300)	(Product : MSM51V4400/L/SL-xxSJ)
26/20-Pin 300 mil plastic TSOP	(TSOP26/20-P-300-K)	(Product : MSM51V4400/L/SL-xxTS-K)
	(TSOP26/20-P-300-L)	(Product : MSM51V4400/L/SL-xxTS-L)

 xx indicates speed rank.

### PRODUCT FAMILY

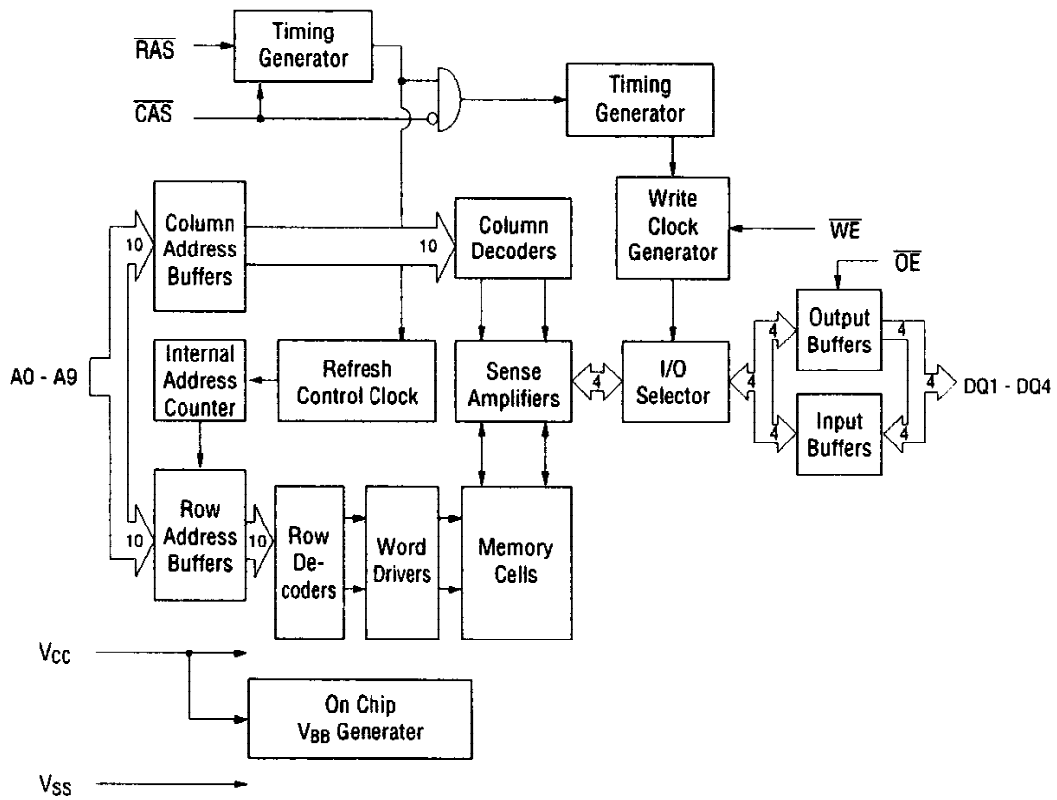
Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	$t_{\text{RAC}}$	$t_{\text{AA}}$	$t_{\text{CAC}}$	$t_{\text{OEA}}$		Operating (Max.)	Standby (Max.)
MSM51V4400/L/SL-60	60 ns	30 ns	15 ns	15 ns	110 ns	252 mW	1.8 mW/ 0.54 mW (L/SL version)
MSM51V4400/L/SL-70	70 ns	35 ns	20 ns	20 ns	130 ns	234 mW	
MSM51V4400/L/SL-80	80 ns	40 ns	20 ns	20 ns	150 ns	216 mW	
MSM51V4400/L/SL-10	100 ns	50 ns	25 ns	25 ns	180 ns	198 mW	

**PIN CONFIGURATION (TOP VIEW)**



Pin Name	Function
A0 - A9	Address Input
RAS	Row Address Strobe
CAS	Column Address Strobe
DQ1 - DQ4	Data Input/Data Output
OE	Output Enable
WE	Write Enable
Vcc	Power Supply (3.3 V)
Vss	Ground (0 V)

**BLOCK DIAGRAM**



**ELECTRICAL CHARACTERISTICS****Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to $V_{SS}$	$V_T$	-0.5 to 4.6	V
Short Circuit Output Current	$I_{OS}$	50	mA
Power Dissipation	$P_D^*$	1	W
Operating Temperature	$T_{opr}$	0 to 70	°C
Storage Temperature	$T_{stg}$	-55 to 150	°C

\*:  $T_a = 25^\circ\text{C}$ **Recommended Operating Conditions** $(T_a = 0^\circ\text{C to } 70^\circ\text{C})$ 

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{CC}$	3.0	3.3	3.6	V
	$V_{SS}$	0	0	0	V
Input High Voltage	$V_{IH}$	2.0	—	$V_{CC} + 0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	—	0.8	V

**Capacitance** $(V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, T_a = 25^\circ\text{C}, f = 1 \text{ MHz})$ 

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9)	$C_{IN1}$	—	6	pF
Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ )	$C_{IN2}$	—	7	pF
Output Capacitance (DQ1 - DQ4)	$C_{I/O}$	—	7	pF

DC Characteristics

(V<sub>CC</sub> = 3.3 V ± 0.3 V, T<sub>a</sub> = 0°C to 70°C)

Parameter	Symbol	Condition	MSM51V4400 /L/SL-60		MSM51V4400 /L/SL-70		MSM51V4400 /L/SL-80		MSM51V4400 /L/SL-10		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -2.0 mA	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.0 mA	0	0.4	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I <sub>LI</sub>	0 V ≤ V <sub>I</sub> ≤ V <sub>CC</sub> + 0.3 V, All other pins not under test = 0 V	-10	10	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I <sub>LO</sub>	DQ disable 0 V ≤ V <sub>O</sub> ≤ V <sub>CC</sub>	-10	10	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I <sub>CC1</sub>	RAS, CAS cycling, t <sub>RC</sub> = Min.	—	70	—	65	—	60	—	55	mA	1, 2
Power Supply Current (Standby)	I <sub>CC2</sub>	RAS, CAS = V <sub>IH</sub>	—	2	—	2	—	2	—	2	mA	1
		RAS, CAS ≥ V <sub>CC</sub> - 0.2 V	—	0.5	—	0.5	—	0.5	—	0.5	μA	1, 5
			—	150	—	150	—	150	—	150	μA	
Average Power Supply Current (RAS-only Refresh)	I <sub>CC3</sub>	RAS cycling, CAS = V <sub>IH</sub> , t <sub>RC</sub> = Min.	—	70	—	65	—	60	—	55	mA	1, 2
Power Supply Current (Standby)	I <sub>CC5</sub>	RAS = V <sub>IH</sub> , CAS = V <sub>IL</sub> , DQ = enable	—	2	—	2	—	2	—	2	mA	1
Average Power Supply Current (CAS before RAS Refresh)	I <sub>CC6</sub>	RAS cycling, CAS before RAS	—	70	—	65	—	60	—	55	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I <sub>CC7</sub>	RAS = V <sub>IL</sub> , CAS cycling, t <sub>PC</sub> = Min.	—	55	—	50	—	45	—	40	mA	1, 3
Average Power Supply Current (Battery Backup)	I <sub>CC10</sub>	t <sub>RC</sub> = 125 μs, CAS before RAS, t <sub>RAS</sub> ≤ 1 μs	—	250	—	250	—	250	—	250	μA	1, 2, 4, 5
Average Power Supply Current (CAS before RAS Self-Refresh)	I <sub>CC5</sub>	RAS ≤ 0.2 V CAS ≤ 0.2 V	—	200	—	200	—	200	—	200	μA	1, 5

- Notes :
1. I<sub>CC</sub> Max. is specified as I<sub>CC</sub> for output open condition.
  2. Address can be changed once or less while RAS = V<sub>IL</sub>.
  3. Address can be changed once or less while CAS = V<sub>IH</sub>.
  4. V<sub>CC</sub> - 0.2 V ≤ V<sub>IH</sub> ≤ 4.6 V, -0.3 V ≤ V<sub>IL</sub> ≤ 0.2 V.
  5. L/SL version.

## AC Characteristics (1/2)

(V<sub>CC</sub> = 3.3 V ±0.3 V, T<sub>a</sub> = 0°C to 70°C) Note 1, 2, 3, 11, 12

Parameter	Symbol	MSM51V4400 /L/SL-60		MSM51V4400 /L/SL-70		MSM51V4400 /L/SL-80		MSM51V4400 /L/SL-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
		Random Read or Write Cycle Time	t <sub>RC</sub>	110	—	130	—	150	—		
Read Modify Write Cycle Time	t <sub>RWC</sub>	150	—	180	—	200	—	240	—	ns	
Fast Page Mode Cycle Time	t <sub>PC</sub>	40	—	45	—	50	—	60	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t <sub>PRWC</sub>	80	—	95	—	100	—	120	—	ns	
Access Time from RAS	t <sub>RAC</sub>	—	60	—	70	—	80	—	100	ns	4, 5, 6
Access Time from CAS	t <sub>CAC</sub>	—	15	—	20	—	20	—	25	ns	4, 5
Access Time from Column Address	t <sub>AA</sub>	—	30	—	35	—	40	—	50	ns	4, 6
Access Time from CAS Precharge	t <sub>CPA</sub>	—	35	—	40	—	45	—	55	ns	4
Access Time from OE	t <sub>OEA</sub>	—	15	—	20	—	20	—	25	ns	4
Output Low Impedance Time from CAS	t <sub>CLZ</sub>	0	—	0	—	0	—	0	—	ns	4
CAS to Data Output Buffer Turn-off Delay Time	t <sub>OFF</sub>	0	15	0	20	0	20	0	25	ns	7
OE to Data Output Buffer Turn-off Delay Time	t <sub>OEZ</sub>	0	15	0	20	0	20	0	25	ns	7
Transition Time	t <sub>T</sub>	3	50	3	50	3	50	3	50	ns	3
Refresh Period	t <sub>REF</sub>	—	16	—	16	—	16	—	16	ms	
Refresh Period (L/SL version)	t <sub>REF</sub>	—	128	—	128	—	128	—	128	ms	
RAS Precharge Time	t <sub>RP</sub>	40	—	50	—	60	—	70	—	ns	
RAS Pulse Width	t <sub>RAS</sub>	60	10,000	70	10,000	80	10,000	100	10,000	ns	
RAS Pulse Width (Fast Page Mode)	t <sub>RASP</sub>	60	100,000	70	100,000	80	100,000	100	100,000	ns	
RAS Hold Time	t <sub>RSH</sub>	15	—	20	—	20	—	25	—	ns	
RAS Hold Time referenced to OE	t <sub>ROH</sub>	15	—	20	—	20	—	25	—	ns	
CAS Precharge Time (Fast Page Mode)	t <sub>CP</sub>	10	—	10	—	10	—	10	—	ns	
CAS Pulse Width	t <sub>CAS</sub>	15	10,000	20	10,000	20	10,000	25	10,000	ns	
CAS Hold Time	t <sub>CSH</sub>	60	—	70	—	80	—	100	—	ns	
CAS to RAS Precharge Time	t <sub>CRP</sub>	5	—	5	—	5	—	5	—	ns	
CAS to RAS Precharge Time	t <sub>RHCP</sub>	35	—	40	—	45	—	50	—	ns	
RAS to CAS Delay Time	t <sub>RCD</sub>	20	45	20	50	20	60	25	75	ns	5
RAS to Column Address Delay Time	t <sub>RAD</sub>	15	30	15	35	15	40	20	50	ns	6
Row Address Set-up Time	t <sub>ASR</sub>	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t <sub>RAH</sub>	10	—	10	—	10	—	15	—	ns	
Column Address Set-up Time	t <sub>ASC</sub>	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t <sub>CAH</sub>	15	—	15	—	15	—	20	—	ns	
Column Address Hold Time from RAS	t <sub>AR</sub>	50	—	55	—	60	—	75	—	ns	
Column Address to RAS Lead Time	t <sub>RAL</sub>	30	—	35	—	40	—	50	—	ns	

AC Characteristics (2/2)

(V<sub>CC</sub> = 3.3 V ±0.3 V, T<sub>a</sub> = 0°C to 70°C) Note 1, 2, 3, 11, 12

Parameter	Symbol	MSM51V4400 /L/SL-60		MSM51V4400 /L/SL-70		MSM51V4400 /L/SL-80		MSM51V4400 /L/SL-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
		Read Command Set-up Time	t <sub>RCS</sub>	0	—	0	—	0	—		
Read Command Hold Time	t <sub>RCH</sub>	0	—	0	—	0	—	0	—	ns	8
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t <sub>RRH</sub>	0	—	0	—	0	—	0	—	ns	8
Write Command Set-up Time	t <sub>WCS</sub>	0	—	0	—	0	—	0	—	ns	9
Write Command Hold Time	t <sub>WCH</sub>	10	—	10	—	10	—	15	—	ns	
Write Command Hold Time from $\overline{\text{RAS}}$	t <sub>WCR</sub>	45	—	50	—	60	—	75	—	ns	
Write Command Pulse Width	t <sub>WP</sub>	10	—	10	—	10	—	15	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t <sub>OEH</sub>	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t <sub>RWL</sub>	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t <sub>CWL</sub>	15	—	20	—	20	—	25	—	ns	
Data-in Set-up Time	t <sub>DS</sub>	0	—	0	—	0	—	0	—	ns	10
Data-in Hold Time	t <sub>DH</sub>	15	—	15	—	15	—	20	—	ns	10
Data-in Hold Time from $\overline{\text{RAS}}$	t <sub>DHR</sub>	50	—	55	—	60	—	75	—	ns	
$\overline{\text{OE}}$ to Data-in Delay Time	t <sub>OED</sub>	15	—	20	—	20	—	25	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>CWD</sub>	35	—	45	—	45	—	55	—	ns	9
Column Address to $\overline{\text{WE}}$ Delay Time	t <sub>AWD</sub>	50	—	60	—	65	—	80	—	ns	9
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>RWD</sub>	80	—	95	—	105	—	130	—	ns	9
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t <sub>CPWD</sub>	60	—	70	—	75	—	85	—	ns	9
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t <sub>RPC</sub>	5	—	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>CSR</sub>	5	—	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>CHR</sub>	10	—	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Refresh Counter Test)	t <sub>CPT</sub>	30	—	35	—	40	—	50	—	ns	
$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Precharge Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>WRP</sub>	10	—	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$ ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>WRH</sub>	10	—	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Set-up Time (Test Mode)	t <sub>WTS</sub>	10	—	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Hold Time (Test Mode)	t <sub>WTH</sub>	10	—	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ Pulse Width ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t <sub>RASS</sub>	100	—	100	—	100	—	100	—	μs	13
$\overline{\text{RAS}}$ Precharge Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t <sub>RPS</sub>	110	—	130	—	150	—	180	—	ns	13
$\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t <sub>CHS</sub>	40	—	50	—	60	—	70	—	ns	13

- Notes:
1. A start-up delay of 200  $\mu$ s is required after power-up, followed by a minimum of eight initialization cycles ( $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh) before proper device operation is achieved.
  2. The AC characteristics assume  $t_T = 5$  ns.
  3.  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.) are reference levels for measuring input timing signals. Transition times ( $t_T$ ) are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. This parameter is measured with a load circuit equivalent to 1 TTL load and 100 pF. Output timing reference levels are  $V_{OH} = 2.0$  V and  $V_{OL} = 0.8$  V.
  5. Operation within the  $t_{RCD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RCD}$  (Max.) is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (Max.) limit, access time is controlled by  $t_{CAC}$ .
  6. Operation within the  $t_{RAD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RAD}$  (Max.) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (Max.) limit, access time is controlled by  $t_{AA}$ .
  7.  $t_{OFF}$  (Max.) and  $t_{OEZ}$  (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
  8.  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  9.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}$  (Min.), the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If  $t_{CWD} \geq t_{CWD}$  (Min.),  $t_{RWD} \geq t_{RWD}$  (Min.),  $t_{AWD} \geq t_{AWD}$  (Min.) and  $t_{CPWD} \geq t_{CPWD}$  (Min.), the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  10. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in an early write cycle, and to  $\overline{\text{WE}}$  leading edge in an  $\overline{\text{OE}}$  control write cycle or a read modify write cycle.
  11. The test mode is initiated by performing a  $\overline{\text{WE}}$  and  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is a 2-bit parallel test function. CA0 is not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a  $\overline{\text{RAS}}$ -only refresh cycle or a  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle.
  12. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.
  13. Only SL version.

**See ADDENDUM K for AC Timing Waveforms**